REMARKS

Claims 1-38 are pending in the present application.

Claims 1-38 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter " Liencres"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part,

> "a node including an active device, an interface to an inter-node network, a memory, and an address network coupling the active device, the interface, and the memory;...
> wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node;
> wherein the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report." (Emphasis added)

The Examiner asserts Liencres teaches each and every limitation recited in Applicant's claim 1. More particularly, the Examiner asserts Liencres teaches the interface to an internode network as being element 31, an address network coupling the active device the interface and the memory as being element 33. In addition, the Examiner asserts Liencres teaches the remaining limitations at col. 7 "read transactions." Applicant respectfully disagrees with the Examiner's characterization of Liencres and the application of Liencres to Applicant's claims.

Specifically, as illustrated in Fig.3a and 3b of Liencres, element 33 cannot be the address network as recited in Applicant's claim 1 because it only couples the bus controller 31 to the processor cache controller 35. It does not couple the active device, the interface, and the memory as recited in claim 1.

However, the above notwithstanding, Applicant further asserts Liencres does not teach or disclose "in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node" or "the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report," as recited in claim 1.

Liencres discloses at col. 7

> "Read Transactions
> When a memory request by the processor 21 cannot by fulfilled by the data in the processor cache memory 37, the processor cache controller 35 sends a read request packet across the cache bus 33 to the bus cache controller 31. The bus cache controller 31 proceeds to broadcast a corresponding read request packet across the memory bus 25. The read transaction initiated by the bus cache controller 31 consists of two packets: a read request packet sent by the bus cache controller 31 on the memory bus 25 and a read reply packet sent by another device on the memory bus. The read request packet contains the address of the memory requested by the processor cache controller 35 and is broadcast to all entities on the memory bus 25. A device on the memory bus 25 that contains the requested memory address responds to the read request packet with a read reply packet containing the subblock which includes the requested memory address. The read reply packet is generally issued by the main memory 23 except when the desired memory address is "owned" by another processor subsystem 20. In that case, the processor subsystem that owns the subblock must generate a read reply packet with the requested data." (Emphasis added)

From the foregoing, Applicant submits Liencres is teaching the cache controller sending a read request to the bus controller, which broadcasts the read request to all devices on the memory bus. Applicant fails to see how this translates to a report sent by the memory, or the interface ignoring the address packet and sending a coherence message to another node.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

Applicant's claims 14 and 26 recites features that are similar to the features recited in claim 1. Thus Applicant submits claims 14 and 26, along with their respective dependent claims, patentably distinguish over Liencres for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-01601/SJC.

Respectfully submitted,

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